Lecture 10: MultiUser MEMS Process (MUMPS)

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Recap

- Various VLSI based fabrication processes and details
- Some design fundamentals
- Sensors and actuators for MEMS
Today

- Pressure sensor: full fabrication animation
- MUMPS
- Details of PolyMUMPs process
- Design rules
- Ledit software to develop your device by polyMUMPs process
- Examples of the devices made by polyMUMPS
Fabrication steps for a piezoresistive gauge or differential, bulk micromachined pressure sensor (Figure 4.6)

1. Deposit Insulator
2. Diffuse piezoresistors
3. Deposit and pattern material
4. Electrochemical etch of backside cavity
5. Anodic Glass bonding
1: Etch recess cavities in silicon
2: Deposit and pattern 3 masking layers; Anisotropic etch silicon
3: Remove first masking layer; Anisotropic etch silicon
4: Remove second masking layer; Anisotropic etch silicon

Capactive bulk micromachined accelerometer (figure 4.14)
Figure 4.5 Pressure sensor with diffused piezoresistive sense elements
Figure 4.7 A miniature silicon fusion bonded absolute pressure sensor.
MUMP\textsc{s} Process

- Multi User MEMS process
- Company MEMSCAP: offers PolyMUMP\textsc{s}, MetalMUMP\textsc{s}, and SOI MUMP\textsc{s}
- Developed at BSAC (Berkeley Sensors and Actuators Center) in late 80’s

- We will study PolyMUMP\textsc{s} a 3 level polysilicon micromachining process
Cleaned Silicon Wafer

Clean Silicon Wafer
Doping of Phosphorous on silicon wafer

Using Standard diffusion furnace using POCL3 as Dopant source

Prevent charge feed through to substrate from electrostatic devices on the surface
Deposition of *Silicon Nitride* layer of thickness 600nm.

Using Standard LPCVD (Low Pressure Chemical Vapor deposition)

Acts as insulation layer
Deposition of polysilicon film
Thickness 500nm

Using Standard LPCVD
(Low Pressure Chemical Vapor deposition)
Deposition of Photo resist
Thickness 500nm

Spin Coating method

- Clean Silicon Wafer
- Silicon Nitride layer
- Poly0 layer
- Photo resist layer
Masking process
Thickness 500nm

UV Source and Mask

- Clean Silicon Wafer
- Silicon Nitride layer
- Poly0 layer
- Photoresist layer
Masking and Exposure with UV source followed with development of photoresist
Thickness 500nm

- Clean Silicon Wafer
- Silicon Nitride layer
- Poly0 layer
- Photoresist layer
Etching of poly0 layer
Thickness 500nm

Reactive Ion Etching (RIE)

After etching photoresist is stripped in solvent bath
Deposition of PSG (Phosphosilicate Glass) layer
Thickness 2 µm

LPCVD process is used to deposit PSG (1st Oxide Layer) layer this is first sacrificial layer
Lithographic patterning of **DIMPLE**
Depth 750 nm

Wafer is coated with photoresist and second level (DIMPLE) is lithographically patterned. Dimples are reactive ion etched. After etching photoresist is stripped.
Lithographic patterning of ANCHOR1

Wafer is coated with photoresist and second level (ANCHOR1) is lithographically patterned. Anchor1 is reactive ion etched. After etching photoresist is stripped.
Deposition of POLY1 Layer along with PSG hard mask

- Clean Silicon Wafer
- Silicon Nitride layer
- Poly0 layer
- PSG layer (1st Oxide)
- Poly1 Layer
Wafers are recoated with photoresist and third level (Poly1) is lithographically patterned. PSG is first etched to create a hard mask and then poly1 is etched by RIE after etching photoresist and PSG mask are removed.
Deposition of 2\textsuperscript{nd} oxide layer

Second oxide layer 0.75 µm of PSG is deposited on water. This layer is patterned twice to allow contact to both poly1 and substrate layers.
Lithographic patterning of P1_P2_Via Etch

Wafer is coated with photoresist and fifth level (POLY1_POL2_VIA) is lithographically patterned. Unwanted second oxide is etched in RIE, stopping on POLY1 and photoresist is stripped.
Lithographic patterning of using ANCHOR2 Etch

Wafer is coated with photoresist and sixth level (ANCHOR2) is lithographically patterned. Second and first oxide are etched in RIE, stopping on either POLY0 or Nitride and photoresist is stripped.
A 1.5 µm undoped polysilicon layer is deposited followed by 200 nm PSG hard mask layer. The wafers are annealed at 1050°C for one hr and dope the polysilicon and reduce residual stress.
Wafer is coated with photoresist and seventh level (POLY2) is lithographically patterned. PSG hard mask and Poly2 layers are etched in RIE,
Deposition of Metal Layer

Wafer is coated with photoresist and eighth level (METAL) is lithographically patterned. Metal (gold with this adhesion layer) is deposited by lift off patterning.
Releasing a structure

The structure are released by immersing the chip in 49 % HF solution. POLY1 “rotor and POLY2 “hub” are released.
MUMP's Process

- Software Ledit for developing your own designs: Demo
- Some designs in the software
- How they look like after fabrication!!